Codec-PC104 Operating Manual

02 Mar 2010, Rev A5

Signalogic, Inc.
9617 Wendell
Dallas, TX 75243

Table Of Contents

1 Items Included in Codec-PC104 Demo Package

- **1.1 Additional Items Included in Engineering Package**
- **1.2 Additional Documentation**

2 Overview and Important Notes

3 Install and Checkout

- **3.1 Switch and Indicator Descriptions**
- **3.2 General Operating Notes**
- **3.3 RS-422 Interface Signal Assignments**

4 Engineering Test and Checkout

- **4.1 Host Based Digital I/O Test**
- **4.2 Using CCS and JTAG Interface**
- **4.3 Programming Flash EEPROM**
- **4.4 Bitrate Measurement Using Digital Scope**

Appendix A, Wiring and Cabling Diagrams
Appendix B, Example Enclosure Images

1 Items Included in Codec PC104 Demo Package

The Codec-PC104 demo package is intended to:

- Demonstrate small-form factor, DSP-based, high compression rate voice encoding
- Serve as a development system platform for development of application-specific DSP software and host processor software
- Provide an evaluation and measurement PC104 board suitable for production and deployment with little or no modification

Below is an inventory of items included in the standard Codec-PC104 demo package:

1) SigC5xxx-PC104 board, configured with SigC5416 single-DSP and SigSD4 4-channel audio module
2) User Control Panel to set Codec options and monitor operating status
3) PC104 power board (Tri-M HESC-104 or similar power board)
4) External AC adapter and wall plug (12V DC output)

See Figure 1 below for a picture of a Codec-PC104 board set as it should appear after unpacking.

1.1 Additional Items Included in Engineering Package

In an engineering shipment, additional items may be included to allow DSP code development and/or PC host code development.

1) Douglas Electronics 6-DE-FC series (or similar) ISA-PC104 passive adapter with 8 inch cable, allowing PC/104 stack to connect directly to the PC bus, for purposes of running PC based test and utility programs , such as Flash EEPROM programming. The adapter package includes:

   - PC/104 passive adapter
   - 2-piece, 8” ribbon cable (1 piece 64 pin, the other 40 pin)
   - ISA bus extender card

2) RS-422 Loopback “plug” connector for testing purposes

See Appendix B, Codec-PC104 Images, for a picture of both stand-alone PC104 configuration and PC development configuration, with PC104-to-ISA adapter installed.

1.2 Additional Documentation

For standard off-the-shelf Codec-PC104 board and associated DSP and audio modules, the Signalogic C5xxx Hardware Reference Guide (HRG) provides relevant information. A current version of C5xxx HRG is maintained at the following FTP site location:

ftp://ftp.signalogic.com/documentation/Boards/SigC55xx

Figure 1, Codec-PC104 Demo/Development Board Set

Figure 1 above shows the Codec-PC104 board mounted on a power board. The AC adapter connection is visible along the left edge of the power board. AC adapters for Europe, Asia and North/South America are available.

2 Overview and Important Notes

The following notes are very important. Please read the sections below first, before powering up or otherwise using the Codec-PC104 demo / development board set. Please keep these notes in mind at all times!!

1) The "ON" LED (CR1 on the SigC5xx-PC104 board) and the LEDs on the power board may take up to 1 second to light after the Codec-PC104 has been powered up.
2) The CR2 LED on the SigC5xx-PC104 board and the "Status" LED on the Control Panel (see Figures 3-5 below) may take up to 1 second or longer to light, as the Codec-PC104 boots from EEPROM and runs built-in self test routines.
3) *For any reason, do not remove* the SigC54xx DSP module or the SigSD4 audio module from the PC104 board with any LEDs on either of the PC104 boards still lit. Be especially sure to check the lower board in the PC/104 stack for active LED indicators (lower board is power board).

Figure 2 below shows a top view general layout of the SigC5xxx-PC104 board, including key configuration jumpers and relevant I/O headers and connectors.

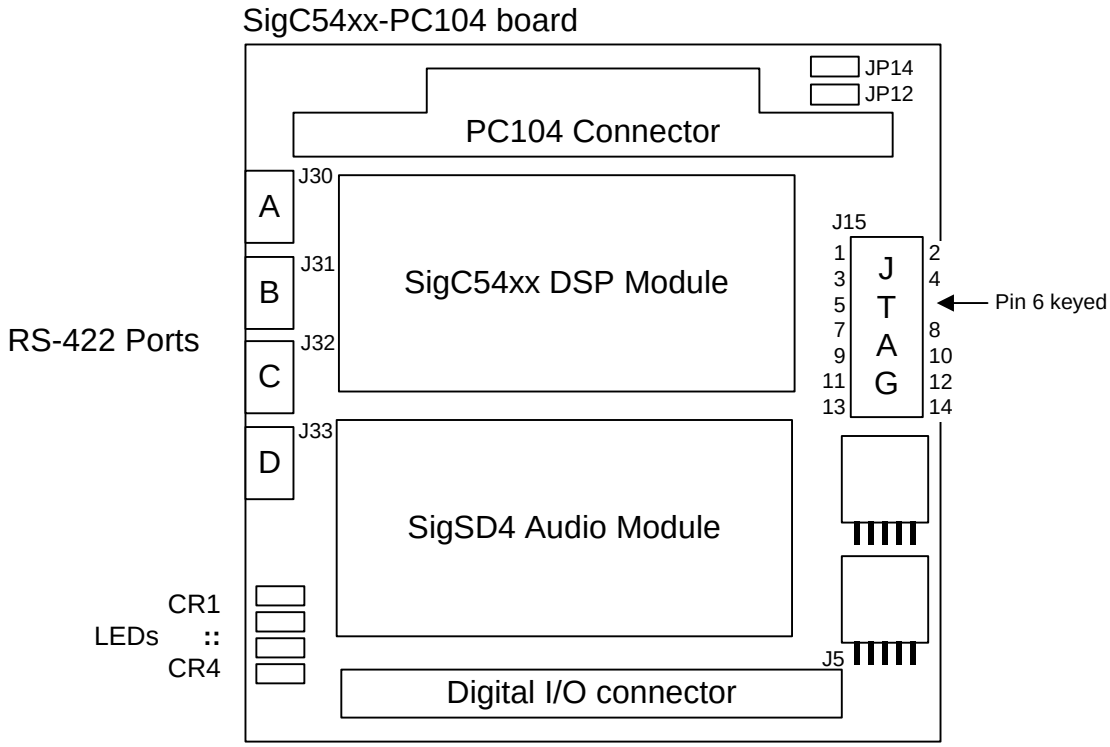


Figure 2, General Layout of SigC5xxx-PC104 Board

If needed, the RS-422 and digital I/O connectors can be fitted with fine-pitch (0.5”) ribbon cables. The Codec-PC104 board set is typically shipped using standard off-the-shelf forms of ribbon cable and mating connectors. If more information is needed about connector and ribbon cable part numbers or more advanced cabling and board-to-board mating techniques is needed, please contact Signalogic.

3 Install and Checkout

Below are instructions for installation and checkout of the Codec-PC104 as shipped by Signalogic. During installation and operation of the Codec-PC104, there are two (2) important notes to keep in mind.

- As shipped by Signalogic, the Codec-PC104 includes a great deal of functionality, but only for test, demo, and checkout purposes. For example, the Mode toggle switch controls Operating Mode vs. Test Mode, but in an actual production unit this switch might control other functionality. There are many other such "demo and test" characteristics of the Codec-PC104.

- The following instructions do not cover engineering and development purposes; they assume the user is not performing DSP code development, and they assume the user is not modifying logic or otherwise making engineering level changes to the PC104 hardware. For engineering instructions, see section 4 below.

Also, please keep in mind that prior to shipment by Signalogic, a Codec-PC104 has minimal undergone vibration and shock testing, but not UL, CE, or other EMC testing. For more information on testing performed at Signalogic prior to shipment, please contact Signalogic.

Codec-PC104 Checkout Instructions

1) First, connect the AC adapter to a 110V or 220V AC outlet. It is recommended that you check the output of the adapter to be approximately 12V in a center-positive format before connecting to the Codec-PC104. This step is important if you are using an AC adapter that did not come with the Codec-PC104 shipment.

2) Connect the AC adapter to the jack marked "DC INPUT" (this jack is usually connected by short sections of black and red wires to the PC104 power board). The power-on indicator LEDs on the power board should light. The "Status" LED on the Codec-PC104 board may take up to 1 second to light.

3) Results of power-on diagnostics and self-tests are shown by LEDs CR1-CR4 on the SigC5xx-PC104 board. For more details, see Section 4, Engineering and Test Checkout.

4) The "Status" LED will light either green in "Run Mode" or rotating from off, green, red, orange in "Test Mode". Run vs. Test Mode is controlled by the Config Mode switch (see notes below).

5) Below is a summary of switch and indicator functionality for the Codec-PC04. For test and check-out, each switch and indicator setting and display should be verified as described below.

The last step in check-out procedure is to make digital scope measurements of clock and framesync signals on the RS-422 header. This step will verify RS-422 port and wiring integrity. See section 4.4 below, Bitrate Measurement Using Digital Scope, for more information.

3.1 Switch and Indicator Descriptions

Below is a summary of switch and LED indicator functionality for the Codec-PC104:

1) Config Mode switch selects:
   - ***Run Mode*** in "Run" position (default mode)
   - ***Test Mode*** in "Test" position (see “Config Mode Notes” below for more information)

Note: on some Codec-PC104 boards, the Config Mode switch may not be installed. In that case, Run Mode is enabled by default.

2) Operating Mode switch selects:
   - Audio Loopback (audio bypass, no speech compression)
   - 2400 bps MELPe
   - 1200 bps MELPe
   - 600 bps MELPe-Plus
   - 16000 bps CVSD
   - 16000 bps G726
   - Audio Loopback in all other positions

   Note: MELPe-600 bps is optional, depending on configuration of board that was ordered.

3) Bit Packing switch selects:
   - 54-bit packed format for MELPe 2400 bps, 81-bit packed format for MELPe 1200 bps or 108-bit format for MELPe-Plus 600 bps
   - 9 byte unpacked format for MELPe 2400 bps (9 6-bit coefficients), 14-byte unpacked format for MELPe 1200 bps (13 6-bit coeeficients and 1 3-bit coefficient), or 18-byte unpacked format for MELPe-Plus 600 bps (18 6-bit coefficients)
   - undefined operation in all other positions

Note that in unpacked MELPe formats, bit rates are 3200 and 1659 bps and 800 bps, respectively.

4) Internal Loopback switch selects whether compressed bitstream packets are looped back internally (inside DSP software) or routed to the RS-422 Port A connector.

5) Clock switch selects whether RS-422 port A expects an external clock (clock pin is an input signal) or generates an internal clock (clock pin is an output signal).

Note: on some Codec-PC104 boards, the Clock switch may not be installed. In that case, Port A External Clock is enabled by default.

6) Status LED indicates:

- Green: normal operation
- Flash orange/red briefly while Codec-PC104 board logic and software initializes
- Red: internal error condition
- Rotating colors: Test Mode operation (see Config Mode switch comments above)

7) The "RESET" switch will cause the Codec-PC104 to reset all hardware, reboot FPGA logic and reboot the DSP from Flash EEPROM when depressed and held longer than 1 second. Depressing the RESET switch for a shorter duration has no effect

Figures 3 through 5 below show top and bottom view of Rev A and Rev B Codec-PC104 boards with switches and indicators marked.

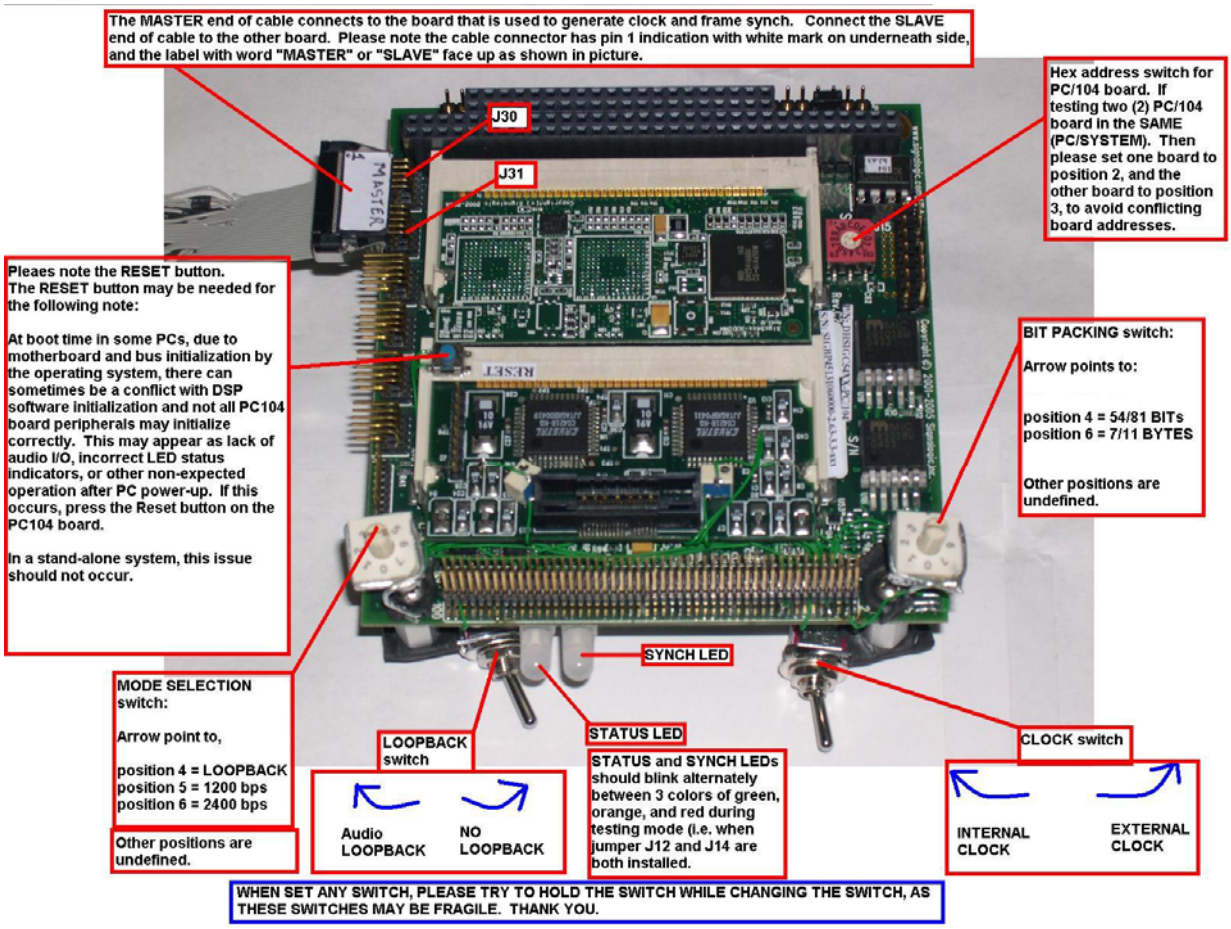

The MASTER end of cable connects to the board that is used to generate clock and frame synch. Connect the SLAVE end of cable to the other board. Please note the cable connector has pin 1 indication with white mark on underneath side, and the label with word "MASTER" or "SLAVE" face up as shown in picture.
J30
J31
Hex address switch for PC/104 board. If testing two (2) PC/104 board in the SAME (PC/SYSTEM). Then please set one board to position 2, and the other board to position 3, to avoid conflicting board addresses.
Pleaes note the RESET button. The RESET button may be needed for the following note:
At boot time in some PCs, due to motherboard and bus initialization by the operating system, there can sometimes be a conflict with DSP software initialization and not all PC104 board peripherals may initialize correctly. This may appear as lack of audio I/O, incorrect LED status indicators, or other non-expected operation after PC power-up. If this occurs, press the Reset button on the PC104 board.
In a stand-alone system, this issue should not occur.
BIT PACKING switch:
Arrow points to:
position 4 = 54/81 BITs
position 6 = 7/11 BYTES
Other positions are undefined.
SYNCH LED
MODE SELECTION switch:
Arrow point to,
position 4 = LOOPBACK
position 5 = 1200 bps
position 6 = 2400 bps
Other positions are undefined.
LOOPBACK switch
Audio LOOPBACK
NO LOOPBACK
STATUS LED
STATUS and SYNCH LEDs should blink alternately between 3 colors of green, orange, and red during testing mode (i.e. when jumper J12 and J14 are both installed.
CLOCK switch
INTERNAL CLOCK
EXTERNAL CLOCK
WHEN SET ANY SWITCH, PLEASE TRY TO HOLD THE SWITCH WHILE CHANGING THE SWITCH, AS THESE SWITCHES MAY BE FRAGILE. THANK YOU.

Figure 3, Rev A Codec-PC104 Board Switches and Indicators, Top View

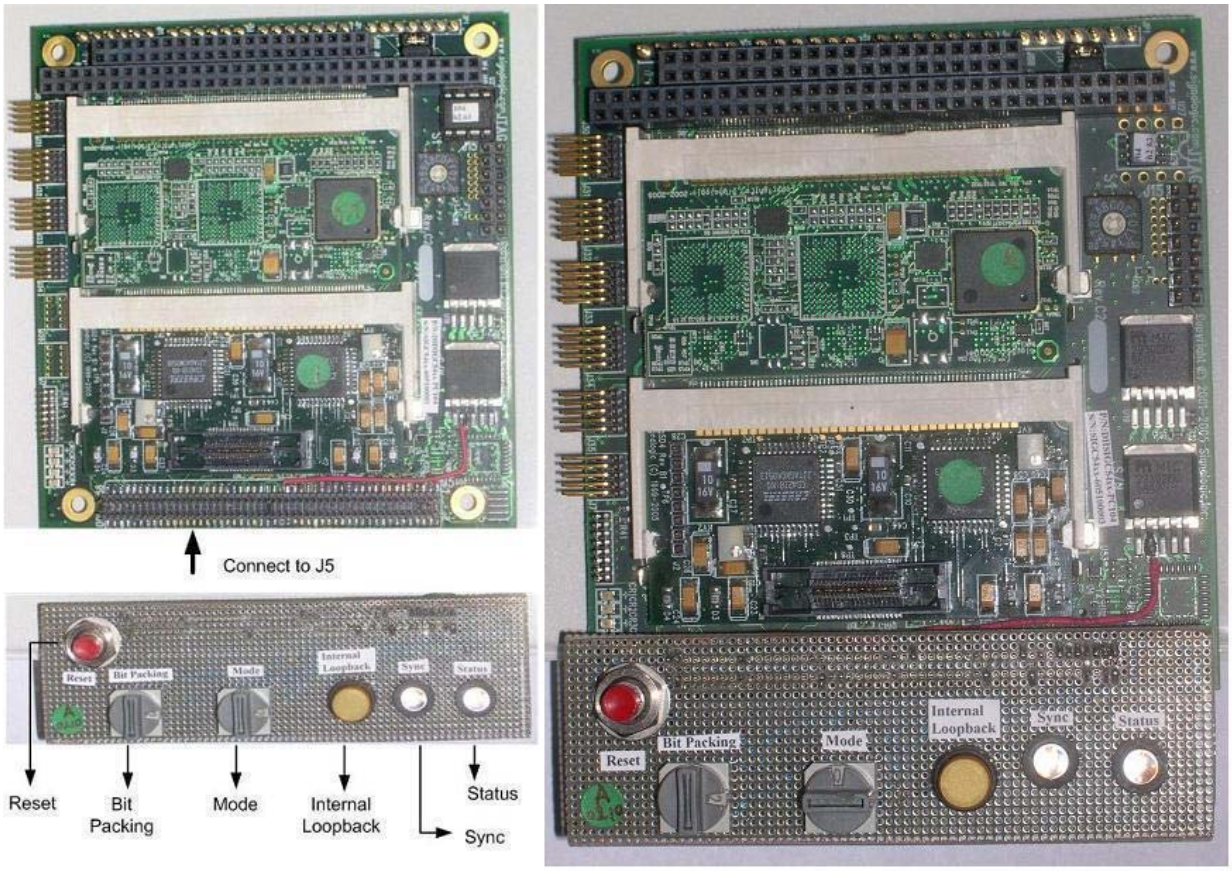


Figure 4, Rev B Codec-PC104 Board Switches and Indicators, Top View

Note that Rev B Codec-PC104 boards use a separate "Control Panel" that connects to the J5 I/O header on the SigC54xx-PC104 board, as shown in Figure 4 above.

Rev B Codec-PC104 Board "Mode" switch positions

Position	Function	Comments
0	G726 16 kbps	
1	CVSD 16 kbps	
2	Audio Loopback	16-bit PCM
3	MELPe 2400 bps	
4	CVSD 32 kbps	*
5	MELPe 600 bps	*
6	MELPe 1200 bps	
7	G726 32 kbps	*

Rev B Codec-PC104 Board "Bit Packing" switch positions

Position	Function
2	54-bit /81-bit byte-packed format
Other *	Unpacked format (see notes in "Bit Packing" description above)

- Not configured unless specified in customer order.

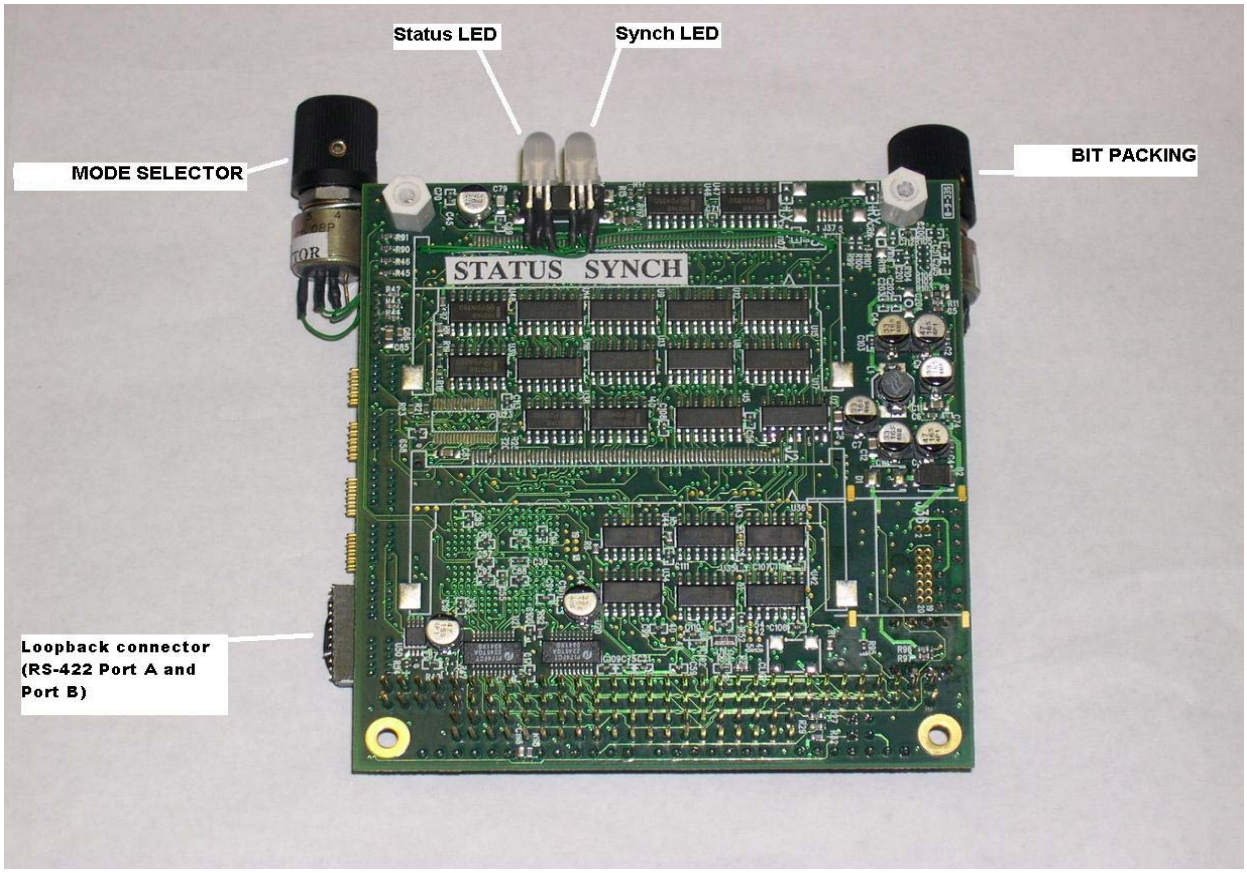


Figure 5, Rev A Codec-PC104 Board Switches and Indicators, Bottom View

Config Mode Notes

1) The default Config Mode position is ***Run Mode*** (switch is in "RUN" position). In Run Mode:

   • When ON, Internal Loopback switch enables internal compressed packet loopback in DSP software. When OFF, packets are routed to RS-422 Port A (J30 header).

   • SYNC1 LED is:

      • off when RS-422 interface is disabled
      • flashing orange/red when sync not obtained yet on RS-422
      • green when sync obtained

   • SYNC2 LED is off

2) ***Test Mode*** occurs when the Config Mode switch is in “TEST” position. In Test Mode:

   • SYNC1 and SYNC2 LEDs rotate through all color/state possibilities (off, green, orange, red). Complete rotation is approx once per second

- changing the position of any control or switch will cause SYNC1 and SYNC2 LEDs to flash green for about 2 sec

Notes:

1. ***On some Codec-PC104 board sets the SYNC2 LED may not be populated.***
2. ***On some Codec-PC104 boards, the Config Mode switch may not be installed. In that case, Run Mode is enabled by default.***

3.2 General Operating Notes

Figure 6 below shows a general view of a test setup, showing audio I/O connections (using a Mictor-to-DB37 breakout cable), a laptop PC generating a speech input (e.g. playing a wav file recording) for compressed speech test purposes, and typical “PC speakers” connected to audio output.

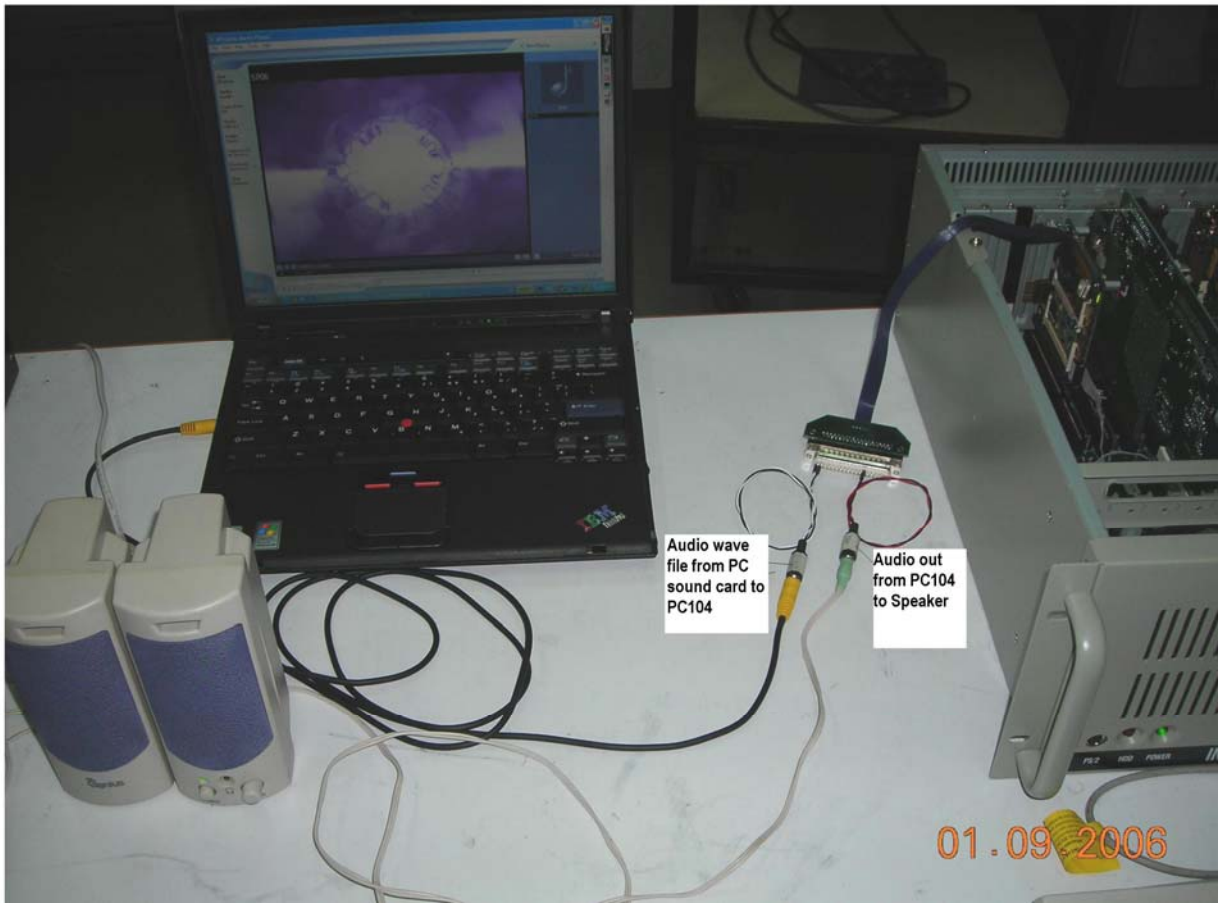


Figure 6, Overall Test Setup

Note that in Figure 6 above, the Codec-PC104 board has been inserted on a PC104-to-ISA passive adapter and placed inside a PC. The passive adapter is an alternative to the stand-alone PC104 power board shown in Figure 1. As the Codec-PC104 boots from an-board Flash EEPROM, either source of power is sufficient as they both provide +5V and -5V. For advanced development purposes, the passive PC adapter can also be used to interface Windows and Linux C/C++ programs to the Codec-PC104.

Figure 7 below shows a close-up view of audio I/O connections, including one channel audio input (differential ended connection) and one channel audio output (single-ended connection).

Note that that Figure 7 shows the Mictor-to-DB37 breakout adapter, with Mictor cable appearing at left and DB37 female header at right. A male DB37 mating connector is also shown, only for purposes of soldering audio wiring.

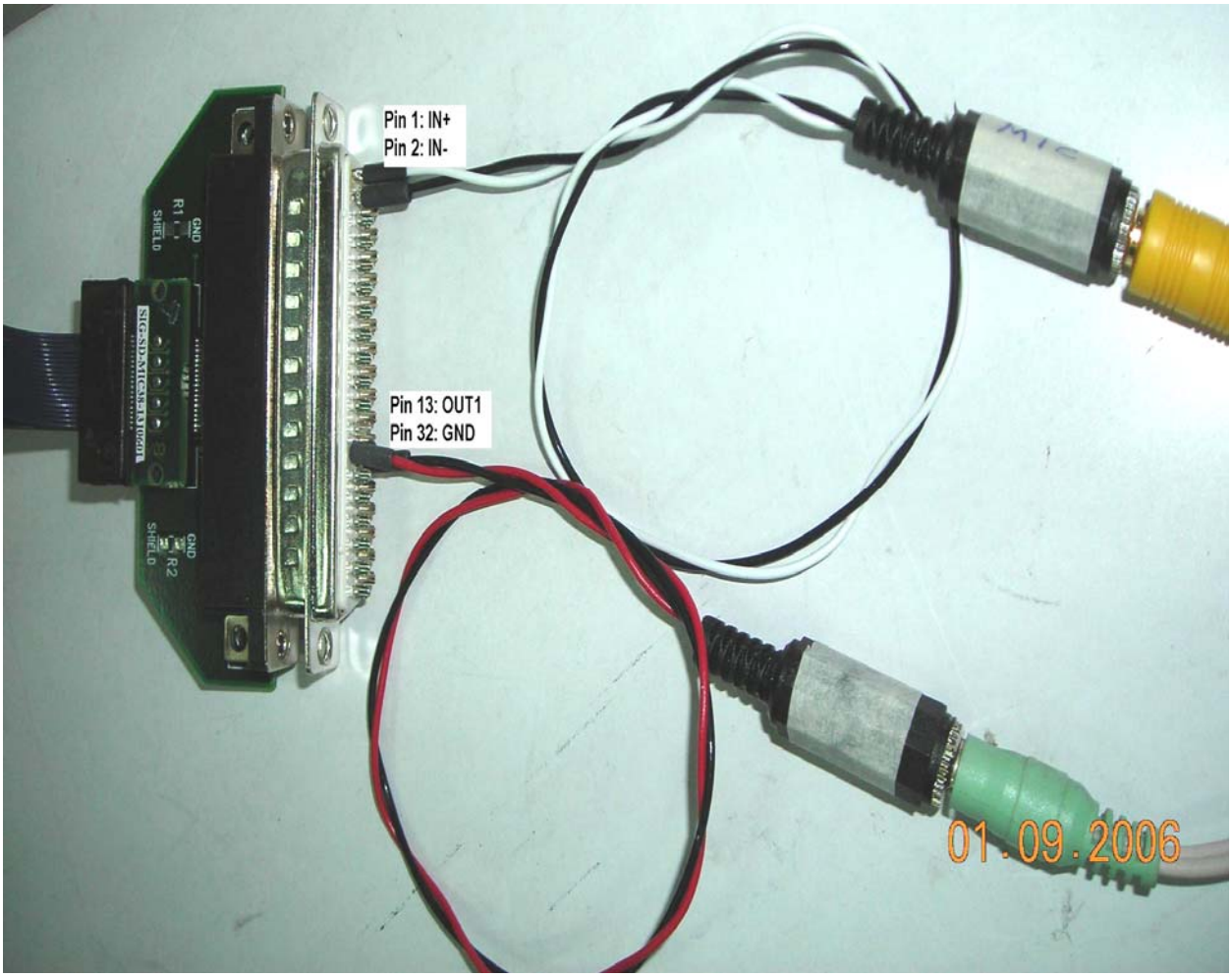


Figure 7, Audio I/O Connections

Below are some general operating notes for the Codec-PC104 board set:

2. When operating mode is changed from 2400 bps to 1200 bps, or from a packed RS-422 format to an unpacked format, it can take a variable amount of time for sync to be re-acquired by the DSP serial transmission algorithm. The longest delay is typically when entering or exiting the 1200 bps unpacked mode.

3. To test sync acquisition across arbitrary bit boundaries, you can remove and re-insert the RS-422 loopback plug connector at random intervals.

4. When sync is not acquired, you should hear a sort of “helicopter noise”. If you think the Codec-PC104 should be transmitting intelligible speech, but instead you hear something else, check the RS-422 loopback plug connector to be sure it is securely inserted and any wires soldered to it are securely attached.

5. Some AC adapters provided with the Codec-PC104 appear to not be fully surge-resistant and a new adapter will be specified at some point. For example, a surge through the ac power (e.g. building air conditioner turns on, outdoor thunderstorm, etc) can cause the –5V internal power to enter an oscillatory, erratic state. The effect is a sudden level drop and hiss in the audio output. +5V and 3.3V seems Ok. Other equipment (PCs, dig scope, etc) plugged into the same ac circuits appear to be resistant to the same surges.

3.3 RS-422 Interface Signal Assignments

This section covers several combinations of RS-422 interface connection, including:

- External Loopback, using “dummy plug”
- Two Codec-PC104 boards, connected back-to-back
- Codec-PC104 board connected to an arbitrary RS-422 terminal

The default Codec-PC104 DSP code uses RS-422 port B (J31 header) to generate framesync and clock signals, and configures RS-422 port A (J30 header) for external clock and framesync signals (i.e. Port A clock and framesync configured as inputs). This is shown in Figure 8 below.

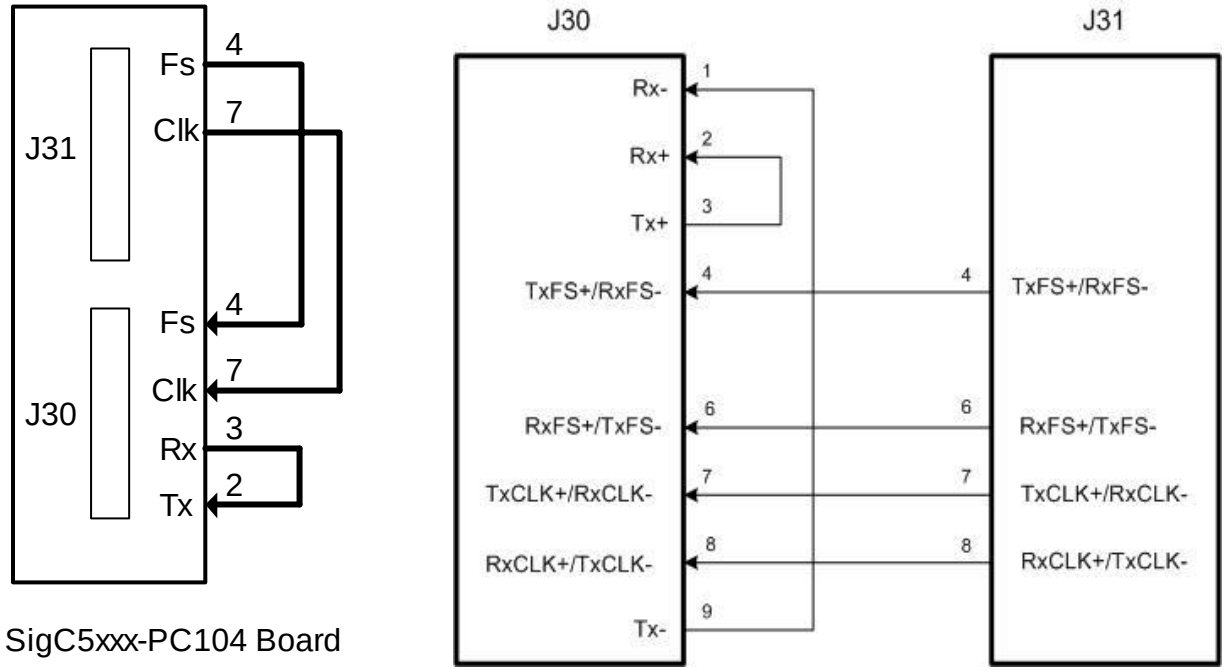


Figure 8, RS-422 External Loopback

The “dummy loopback plug” shipped with Codec-PC104 demo and development systems, when installed across the J30 and J31 headers, assumes “Port B as master” configuration shown above and allows external loopback of compressed bitstream data. Note that the Internal Loopback switch, which controls internal DSP software loopback, must be OFF for RS-422 Port A to transmit and receive data.

For MELPe codecs, when the loopback plug is first connected, it can take from 1 to 20 sec for the sync acquisition algorithm to fully regain sync. Typically sync is regained 2-3 sec, but can take longer especially at 600 bps with unusual combinations of serial framesync alignment with previous buffer data still stored in DSP memory. This also applies when the RS-422 connection is broken and then re-connected. For CVSD, G726 and other ADPCM codecs, sync is obtained

instantaneously – this is because ADPCM codec packet sizes are always defined as an integer number of bytes.

Disconnecting and reconnecting the loopback plug header while the Codec-PC104 system continues to run will not damage the RS-422 circuitry and can make an effective “live demo” technique.

Figure 9 below shows recommended connections between two (2) Codec-PC104 boards; i.e. in a back-to-back board configuration.

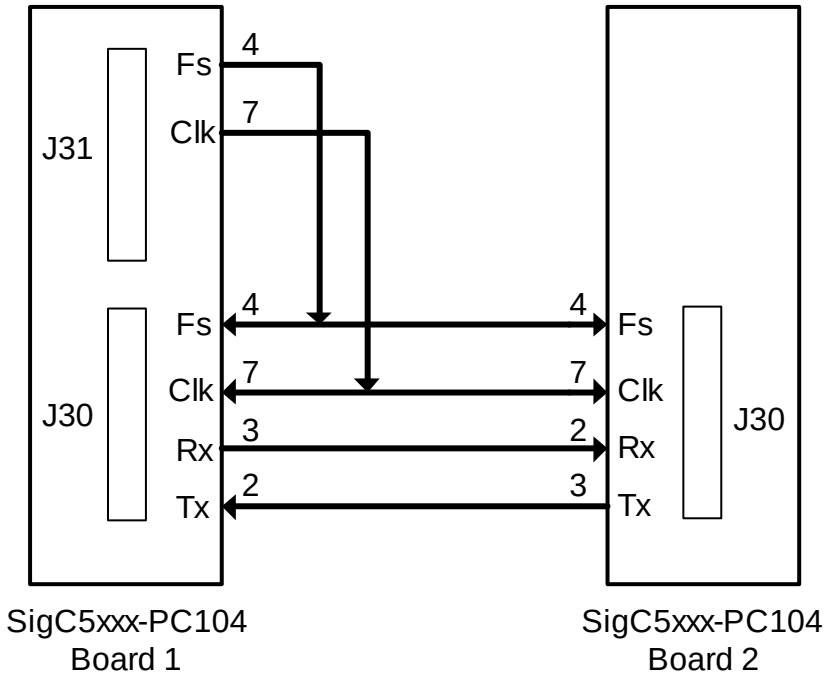


Figure 9, RS-422 Board-to-Board Connection

In Figure 9, Port B on Board #1 is acting as a clock and framesync master, driving port A on both Board #1 and Board #2.

Note that in board-to-board or board-to-terminal situations, it’s important to connect both ± (positive and negative) RS-422 signals. Transmission may function Ok without negative side signals connected, but leaves the interface susceptible to small sources of noise, such as AC power fluctuation, which can cause glitches producing false 1’s or 0’s.

Figure 10 below shows a board-to-terminal connection, with “terminal” implying a voice codec resource with RS-422 interface.

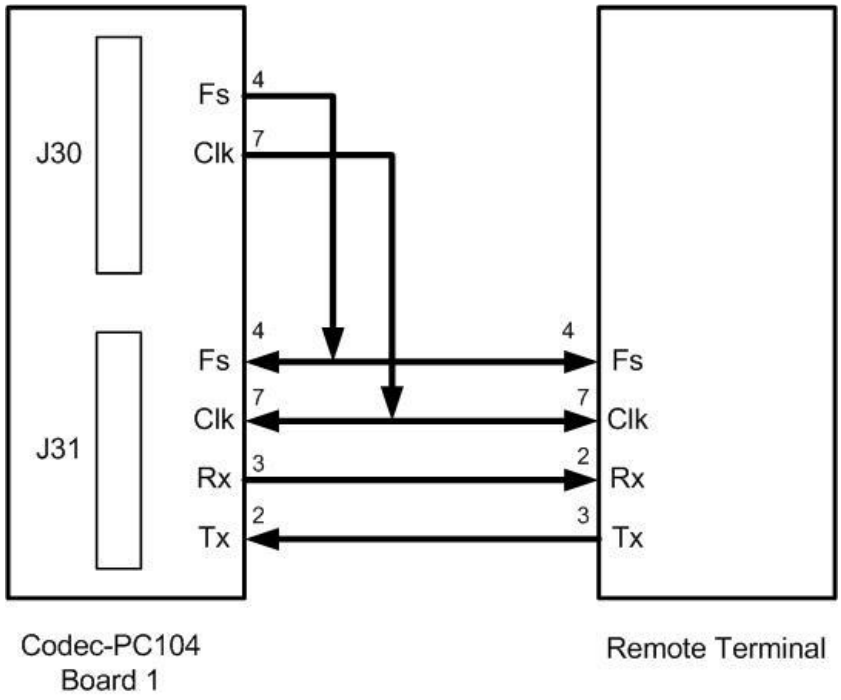


Figure 10, RS-422 Board-to-Terminal Connection

Note also that use of Port B is not required. Clock and framesync signals may be supplied from any source, as long as clock rate matches the selected algorithm bitrate (e.g. 2400, 1200, or 600 bps for byte-packed modes), and framesync rate is equal to the clock rate divided by 8.

If Port A should become a master for clock and framesync signals; i.e. these signals should be defined as outputs, then run-time DSP C code initialization must be changed. See section 4.2 below, Using CCS with JTAG Interface, for more information about modifying and rebuilding DSP code using Texas Instruments development tools.

4 Engineering Test and Checkout

Below are instructions for engineering test and checkout.

1) Separate the power supply PC104 board from the SigC5xxx PC104 board. When used in an engineering and development configuration, the power board is not used.
2) Install the SigC5xxx-PC104 board on the adapter card.
3) Insert the combined SigC5xxx-PC104 board plus adapter into the PC ISA slot, as shown in Figure 11 below. *Make sure power to the PC is off first!!!*

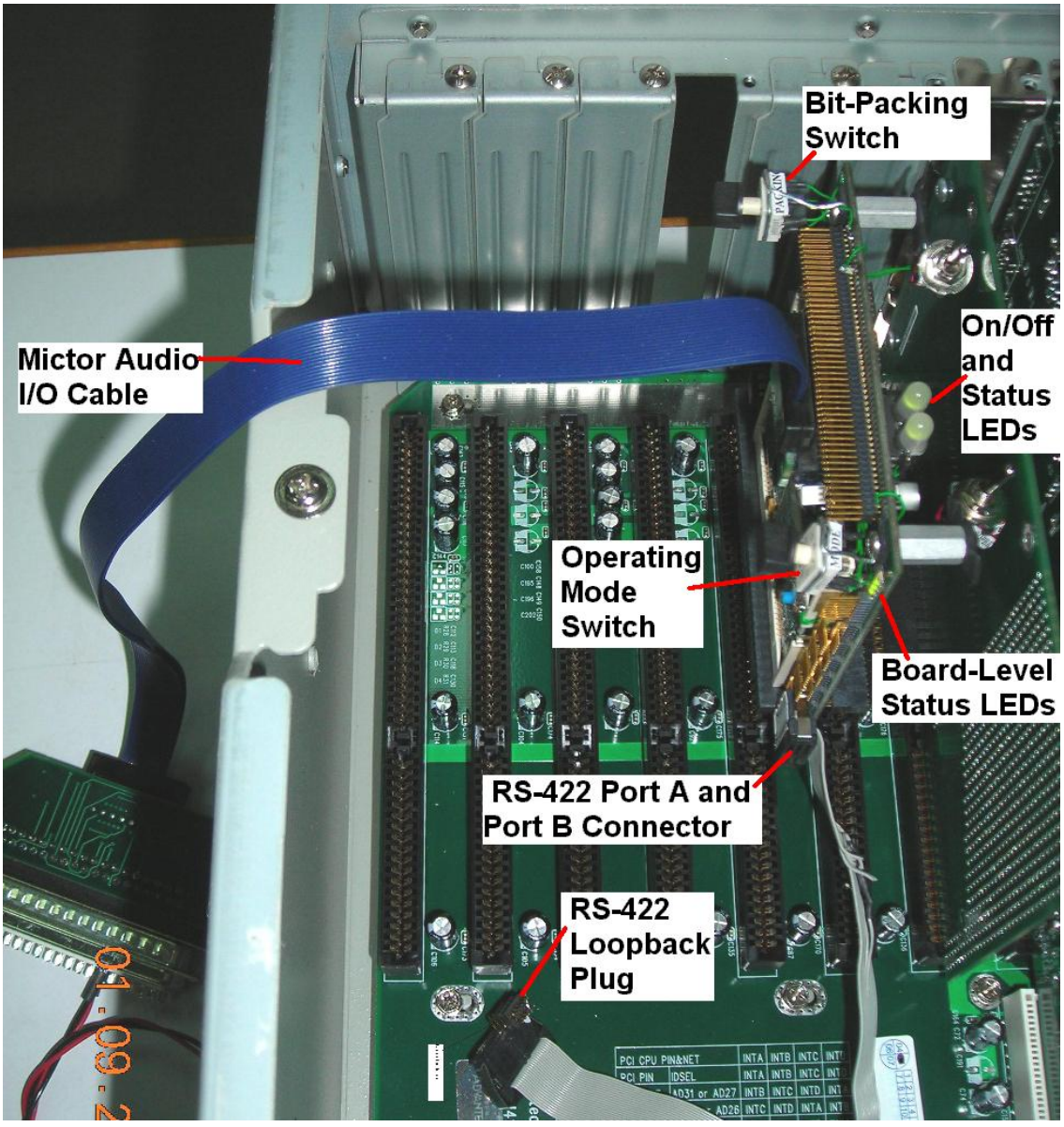


Figure 11, SigC5xx-PC104 Board Installed on ISA-to-PC104 Adapter

Note: when installing the SigC5xxx-PC104 board on the PC104-to-ISA adapter, make absolutely sure all pin alignment is correct, and there is no 'off by one pin" situation, which can lead to destructive damage of the PC104 board, PC motherboard, or both.

4) Turn on the PC. Make sure the SigC5xxx-PC104 board has powered up correctly (see comments about power board and "Status" LED sequence in Section 3 above, Install and Checkout). If the SigC5xxx-PC104 board has passed its internal self-tests and stand-alone mode initialization, LEDs CR1 and CR2 should light (see Figure 11 above). CR1 lit indicates the logic controller in the Codec-PC104 board has booted correctly and internal self-tests have completed successfully. CR2 lit indicates that stand-alone mode initialization have completed correctly, including DSP code boot from Flash EEPROM.

Note that the SigC5xxx-PC104 board can boot either in "stand-alone mode" or "host mode". In stand-alone mode, the board boots from onboard Flash; i.e. DSP code is loaded from the Flash. In host mode, DSP code must be downloaded in one of two ways:

- from a host program such as Hypersignal-Macro or Visual Studio or .NET program using DirectDSP libraries

- using Code Composer Studio integrated development environment (from Texas Instruments) plus JTAG development tools (see section 4.2 below, Using CCS with JTAG Interface)

The boot mode is selected by JP12 (see Figure 2 above, General Layout of SigC5xxx-PC104 Board). If JP12 is inserted, then stand-alone mode boot is selected, and the CR2 LED can be used to monitor stand-alone boot status. If the CR2 LED is lit after the board is turned on, then stand-alone mode initialization and DSP code boot were accomplished successfully.

Note that if stand-alone mode is enabled, voice codec functionality, including user I/O switches and LED indicators, should be operational immediately after boot.

Note also that CR3 will be lit if a motherboard is detected, either as a host processor board in the PC104 stack, or a PC motherboard when using the ISA-to-PC104 adapter. If CR3 is not lit, then the SigC5xxx-PC104 onboard logic will assume it can enable bus master access to other PC104 boards in the stack such as additional RS-232 or other I/O.

4.1 Host Based Digital I/O Test

Below are instructions to perform a full digital I/O test. Note that you must have the PC104-to-ISA adapter installed as described in section 4 above, Engineering Test and Checkout.

The host based digital I/O test program allows each control to be tested individually, independent of DSP code. This test is used at Signalogic as the equivalent of a PCB "electrical test" to verify that all controls and indicators are connected properly, there are no opens or shorts between digital I/O lines, and no controls are intermittent.

1) Turn on the PC and run the Digital I/O Test Program (digio_test.exe)

2) Enter option "2" for PC104 board option and press "Enter"

3) Enter option "2" for C54xx and press "Enter"

4) Enter option "2" for Module Site and press "Enter"

5) Enter option "3" for Test Type and press "Enter". You should see a screen display similar to that shown below in Figure 12:

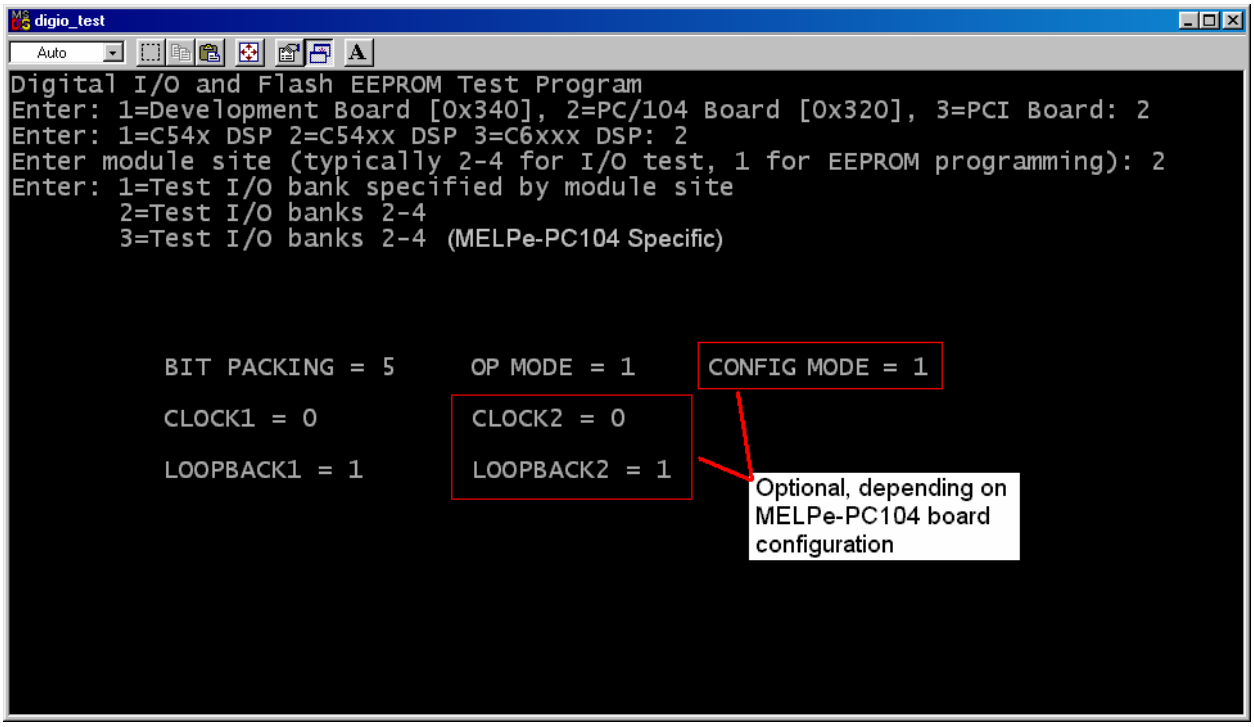

digio_test
Auto
Digital I/O and Flash EEPROM Test Program
Enter: 1=Development Board [0x340], 2=PC/104 Board [0x320], 3=PCI Board: 2
Enter: 1=C54x DSP 2=C54xx DSP 3=C6xxx DSP: 2
Enter module site (typically 2-4 for I/O test, 1 for EEPROM programming): 2
Enter: 1=Test I/O bank specified by module site
2=Test I/O banks 2-4
3=Test I/O banks 2-4 (MELPe-PC104 Specific)
BIT PACKING = 5
OP MODE = 1
CONFIG MODE = 1
CLOCK1 = 0
CLOCK2 = 0
LOOPBACK1 = 1
LOOPBACK2 = 1
Optional, depending on MELPe-PC104 board configuration

Figure 12, Host Based Test Display for SigC5xx-PC104 Digital I/O

6) The "STATUS" and "SYNC" LEDs should start changing colors, going from off to red to green to orange, then back to off again.

7) Flipping the switches will result in changes viewable in the display area of the Digital I/O Test Program. For example, if you toggle the Config Mode switch, you should see a corresponding toggle between “1” and “0” in the screen display shown in Figure 12.

8) After tests have been completed close the Digital I/O Test Program.

9) Power down the PC.

10) Wait for all LEDs to turn off, including any LEDs on the PC motherboard. The PC104-to-ISA adapter can now be safely removed.

4.2 Using CCS with JTAG Interface

Note that this section *does not* assume you have a PC104-to-ISA adapter installed. No host PC connection is required other than a standard JTAG cable, normally supplied by a Spectrum Digital or other similar emulator connected to the PC parallel port or USB port. The JTAG emulator should be connected to J15 on the SigC5xxx-PC104 board (see Figure 2 above).

Code Composer Studio (CCS) DSP software project and executable files are supplied by Signalogic with the Codec-PC104 for demonstration and testing purposes. The Signalogic-provided, default project is called MELPe_Dev and performs 2400 and 1200 bps MELPe processing, including loopback of compressed digital speech via RS-422 port A (J30 header on the SigC5xxx-PC104 board).

The CCS project and source code files provided with the Codec-PC104 are equivalent to a Development License provided by Signalogic. Source code includes high-level C code that performs the following:

- calls MELPe encode and decode functions in a real-time, dual-buffered context
- provides examples of real-time digital I/O that for all Codec-PC104 controls and indicators
- configures SigC5xxx-PC104 base board peripherals, including TDM routing logic, audio I/O, RS-422 I/O, etc

Note that the MELPe_dev.out executable file provided with Codec-PC104s (or re-generated by rebuilding the default MELPe_Dev CCS project) is the same as the program stored in the Flash EEPROM on the SigC5xxx-PC104 board.

To load and run the MELPe_Dev CCS project:

1) Power on the Codec-PC104 as described in section 4 above.
2) Connect to JTAG header J15 on the SigC5xxx-PC104 board using the parallel port of the computer. Note that pin 6 is keyed, per standard TI JTAG convention. See Figure 2 above for orientation of the JTAG header on the SigC5xxx-PC104 board.
3) As a sanity check, run SDConfig and select Reset and EMU Check menu items. This will test the integrity of the JTAG connection and ensure it is secure and operating correctly.
4) Open CCS software on the PC desktop.
5) On the CCS main menu, select Project | Open to open the MELPe_Dev project file

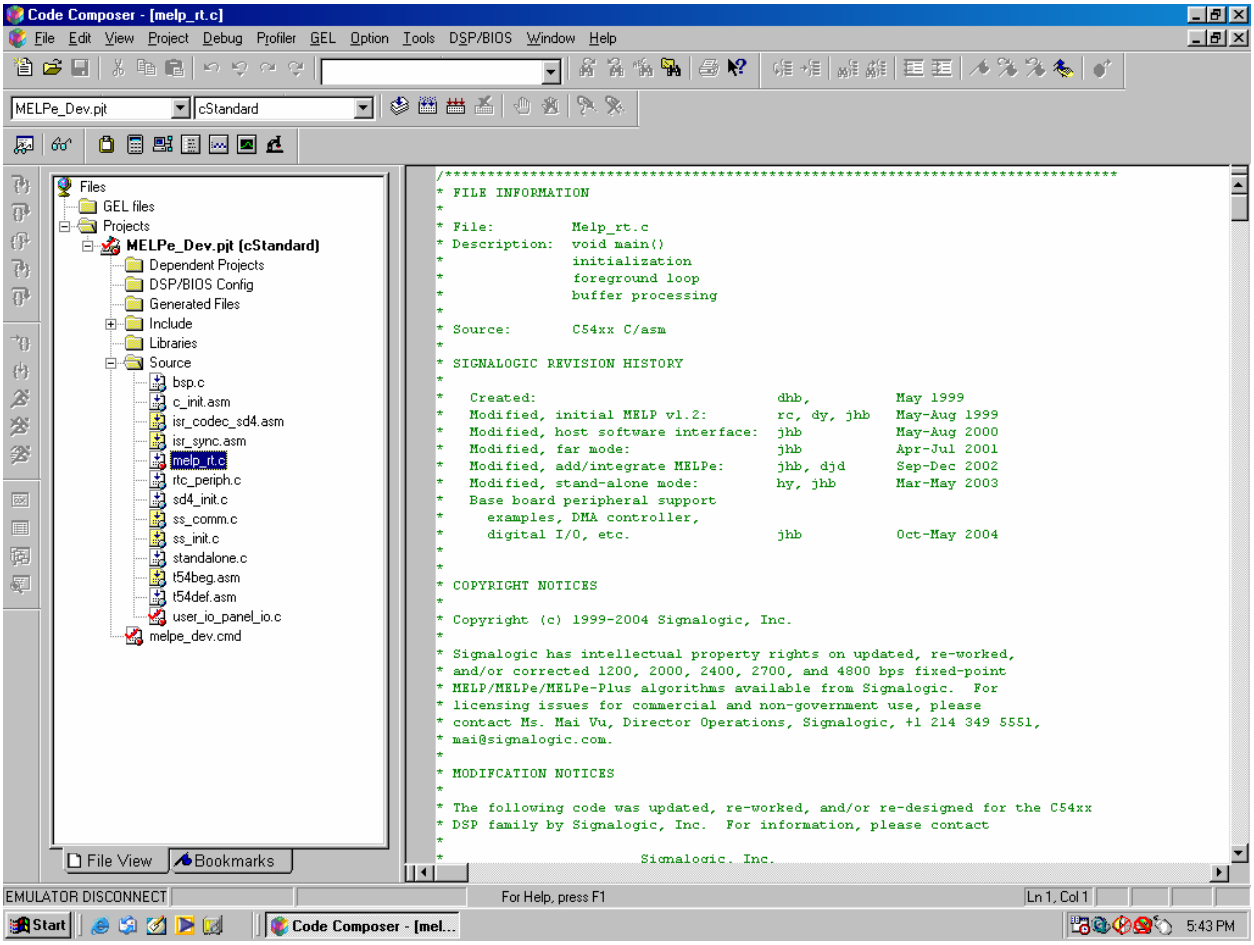


Figure 13, Opening the MELPe_Dev Project in CCS

6) On the CCS main menu, select File | Load Program to load the correct MELPe_Dev.out file through the JTAG interface. Note that after loading once, you can also select File | Reload Program, as shown in Figure 14 below.

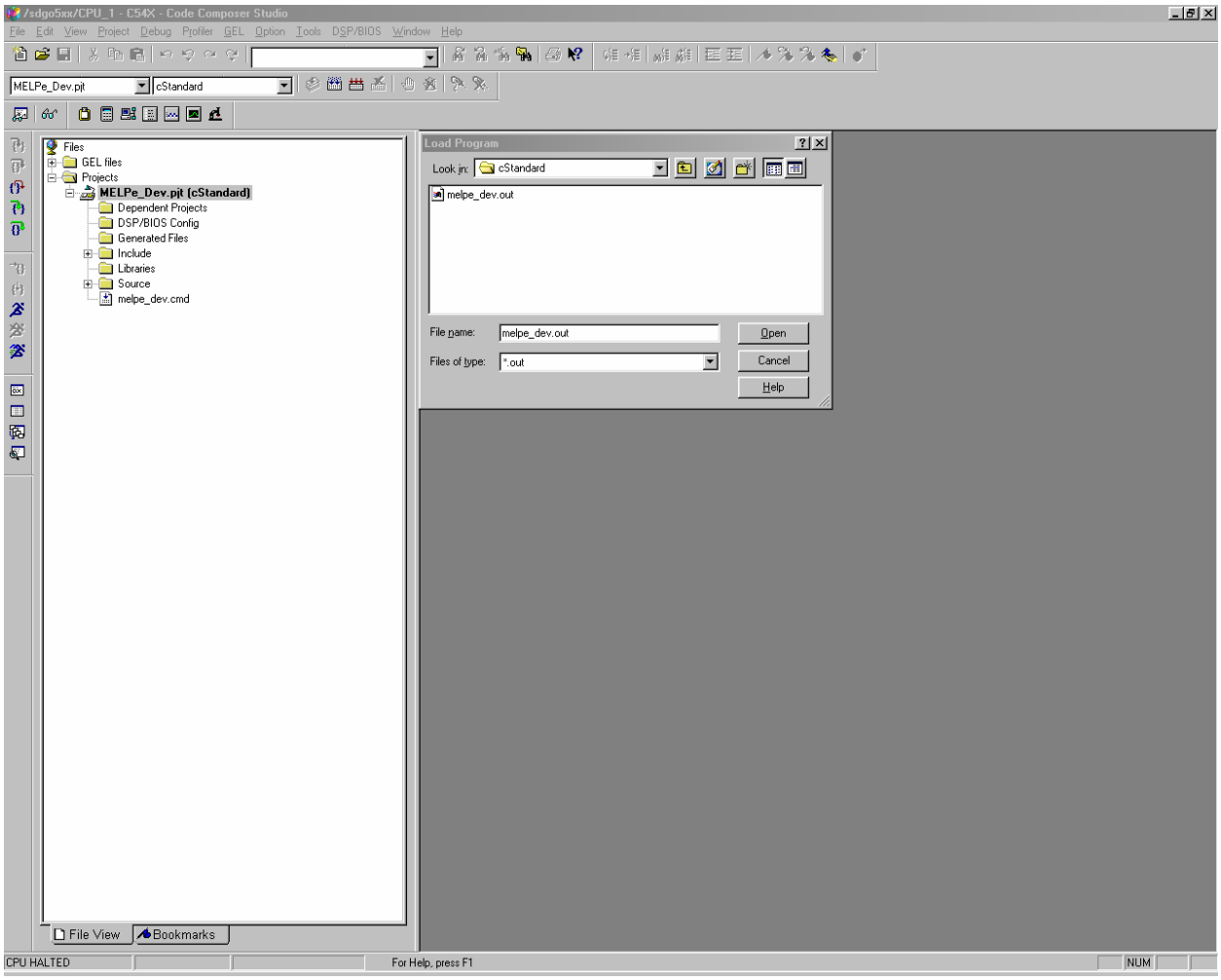


Figure 14, Loading Executable DSP Program via JTAG

7) On the CCS main menu, select Debug | Reset CPU.

8) On the CCS main menu, select Debug | Run

9) At this point, the Codec-PC104 should begin operating. Normal CCS debug functionality such as single-step, breakpoint, etc. should be operational. If you make source code changes, then always follow this procedure:

   a) Save and rebuild the project

   b) Reload the program

   c) Reset CPU

d) Run again

10) Connect audio input and output to the Codec-PC104 as shown in Figure 7 above.

Note that more detailed information about installing, configuring, and using CCS with Signalogic DSP hardware and software is available in the C5xxx Hardware Reference Guide, located at:

ftp://ftp.signalogic.com/documentation/Boards/SigC55xx/

4.3 Programming Flash EEPROM

From time to time, the contents of Flash EEPROM on the SigC5xxx-PC104 board may need to be updated with new DSP executable code. This is typically done infrequently, after periods of development, coding, and test are complete, and prior to shipment to the end-customer.

Below are instructions for running the EEPROM Flash programming utility. These instructions assume the PC104-to-ISA adapter is installed and the Codec-PC104 is correctly powered up and operating, as explained in section 4 above.

1) First make sure the Codec-PC104 is not running MELPe test program or other DSP code. One simple way to do this is to run CCS software (assumes JTAG header is installed), and perform a Reset CPU function.

2) Run mkrom.bat, using one of the examples shown below for different DSP processor types. Note that the .out file used as input in the examples may be named differently, depending on your application and purposes:

   Example for board with C54xx processor(s):

   ```
   mkrom –54 melpe_dev
   ```

   Example for board with C55xx processor(s):

   ```
   mkrom –55 melpe_dev _c_int00
   ```

   The mkrom.bat batch file takes in a .out file created by Texas Inst Code Composer Studio (CCS) software and creates a .rom file. It invokes TI's hex500 "hex conversion" utility (provided with CCS software), using the Tektronix "extended 32-bit addressing" format. 32-bit addressing allows unified support for both C6xxx devices also C5xxx support in cases of loading code into far memory (above 64k). Note that mkrom expects a standard installation of TI tools and CCS software; for example, hex500 should typically be located at:

   ```
   \ti\c5400\cgtools\bin
   ```

   If not, then mkrom.bat can be edited to point to the correct path as needed using a standard text editor.

3) On the host PC, run the digio_test.exe program. At the prompts, enter the following selections:

Entry	Description	Comments
2	Board Type	2 = PC/104 3 = PCI
2	Processor Type	2 = C5xxx 3 = C6xxx
1	Module Site	Module site to be used for initial DSP boot (use 1 for Codec-PC104)
5	Test Type	Flash EEPROM erase, test, and program

The utility will first erase and test the EEPROM, and if no error occurs, it will prompt you for the following:

Prompt	Comments
.rom filename	Either filename or full path can be entered; if only filename, the utility searches on the current subdir and the hsmacro subdir
PMST Value	The PMST register sets memory map, interrupt table, and Overlay mode values for C54xx processors. For C5409 the default value is 0xe0, for C5416 the default value is 0xa8; entry is expected in hex ('0x' may or may not be entered). See additional notes below. For Codec-PC104, use value 0x00a8.
SWWSR	Not currently implemented. Default value in DSP after reset is assumed.
BCSR	Not currently implemented. Default value in DSP after reset is assumed.
Processor Core List	Default value is 1; each bit indicates a core to receive Flash data at boot time and to be released from reset. For example, a core list of 7 would indicate to boot the first 3 cores on the board. For Codec-PC104, use value of 1.

After entering the above prompts, and erasing the Flash EEPROM, the programming utility should proceed to program the Flash EEPROM. This can take a while – up to several minutes -- especially if the DSP executable file is large. Upon completion, you should see a screen display similar to Figure 15 below:

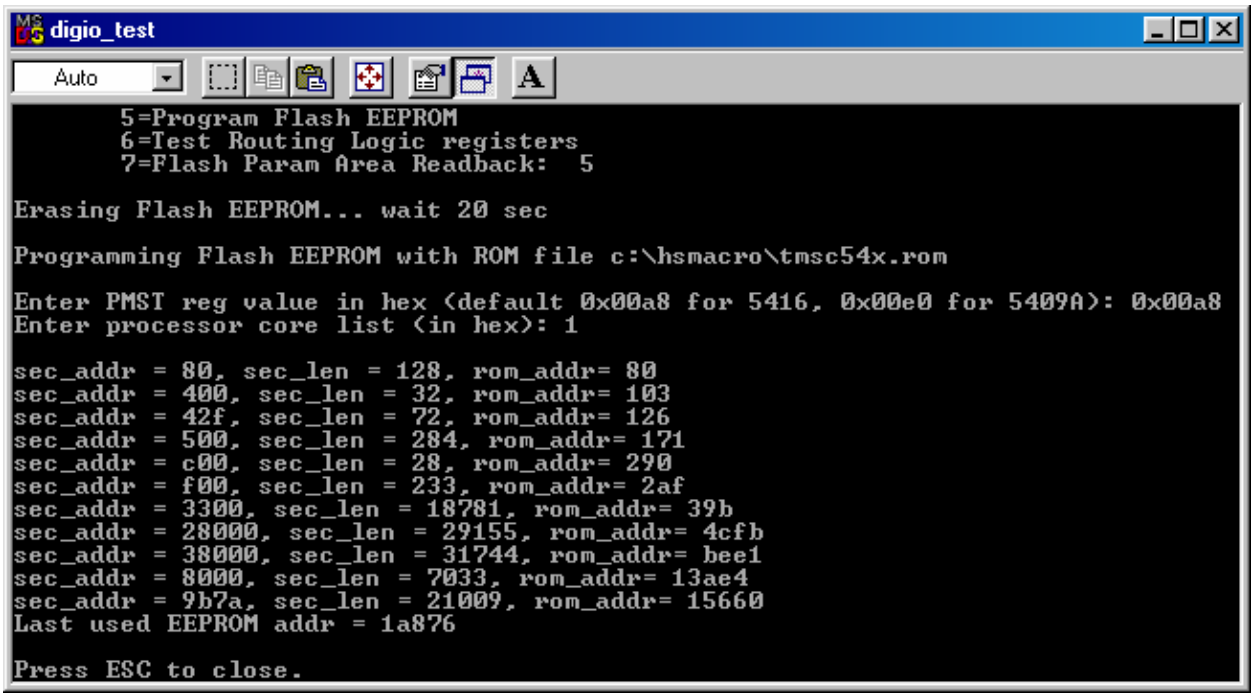

digio_test
Auto
5=Program Flash EEPROM
6=Test Routing Logic registers
7=Flash Param Area Readback: 5
Erasing Flash EEPROM... wait 20 sec
Programming Flash EEPROM with ROM file c:\hsmacro\tmsc54x.rom
Enter PMST reg value in hex (default 0x00a8 for 5416, 0x00e0 for 5409A): 0x00a8
Enter processor core list (in hex): 1
sec_addr = 80, sec_len = 128, rom_addr= 80
sec_addr = 400, sec_len = 32, rom_addr= 103
sec_addr = 42f, sec_len = 72, rom_addr= 126
sec_addr = 500, sec_len = 284, rom_addr= 171
sec_addr = c00, sec_len = 28, rom_addr= 290
sec_addr = f00, sec_len = 233, rom_addr= 2af
sec_addr = 3300, sec_len = 18781, rom_addr= 39b
sec_addr = 28000, sec_len = 29155, rom_addr= 4cfb
sec_addr = 38000, sec_len = 31744, rom_addr= bee1
sec_addr = 8000, sec_len = 7033, rom_addr= 13ae4
sec_addr = 9b7a, sec_len = 21009, rom_addr= 15660
Last used EEPROM addr = 1a876
Press ESC to close.

Figure 15, Flash EEPROM Programming Utility Display Upon Completion

Notes

1. Processor specific prompts only appear depending on the value entered for the initial Processor Type prompt when the programming utility first runs. Shared prompts always appear, regardless of processor type.

2. The programming utility stores the above parameters and others in a separate "header" area in the Flash EEPROM. The header area includes signature data that allows boot logic to detect whether a valid program has been stored in Flash EEPROM. For detailed information on header area format, as well as other EEPROM area format, see section 10.6.4 in the C5xxx Hardware Reference Guide, EEPROM Storage Format.

3. The PMST value should be 0x00e0 for C5409 or C5409A devices, and 0x00a8 for C5416 or C5421 devices. Whatever value you enter in the EEPROM programming utility will be deposited at location 0x3ffc1 in the EEPROM, i.e. the 2nd location of the boot program. The first instruction of the boot program is:

```
PMST = #0xNNNN
```

where NNNN is the value entered in the programming utility prompt.

4. Boot code in t54beg.asm first sets PMST to 0x00e0, and then set back to 0x00a8 if the processor type auto-detection code finds a C5416 or C542x processor.

5. If a far-mode executable file has been used for mkrom input, boot logic will automatically set XHPIA as needed to correctly store data using 24-bit addressing.

6. If you use the Flash EEPROM for non-volatile data storage, for example to store data from a DSP program, it is suggested that data storage start no lower than EEPROM location 0x20000. This will leave ample space for program storage (approx 256k x 16 for C5xxx). In any case, you should be very careful not to overwrite valid EEPROM executable program data. Note that a DSP program can learn the total length of stored program data by reading the section lengths and in the EEPROM until the last length, which will be zero. For more information, see section 10.6.5, Executable DSP Program Storage Format in EEPROM, in the C5xxx Hardware Reference Guide.

Board Configuration and Test

The final step in Flash EEPROM programming is to ensure the SigC5xxx-PC104 board is configured for stand-alone operation, which will cause logic on the board to test the Flash EEPROM for a valid program, verify that auto-detected module type matches the stored program type, and boot the DSP(s) from the Flash EEPROM program. To configure the board for stand-alone operation, jumper JP14 must be inserted.

After verifying JP14 is correctly installed, the board must be reset or run from power-on for the configuration to take effect.

As noted in section 4 above, LEDs CR1 and CR2 should light after power-on or Reset (see Figure 2 above). CR1 indicates whether the logic boot and internal self-tests in the SigC5xxx-PC104 onboard logic controller completed successfully. CR2 indicates whether stand-alone mode initialization – including EEPROM program load and DSP code boot -- completed correctly.

Note that the logic boot LED (CR1) should light first, and the stand-alone boot LED (CR2) should light after the DSP code program is fully transferred from Flash EEPROM to DSP memory. Depending on the size of the executable DSP program, there will be a delay after CR1 illuminates and before CR2 illuminates, typically ranging from 250 msec to about 3/4 sec.

4.4 Bitrate Measurement Using Digital Scope

Below are instructions to measure speech codec output bitrates using a digital oscilloscope. These instructions assume the Codec-PC104 is turned on and operating as noted above. Audio I/O should be connected and it should be possible to verify the Codec-PC104 is working by listening to audio output.

Operate the Codec-PC104 in 1200 or 2400 modes, with either packed or unpacked formats selected, and enable Loopback switch).

Attach channel 1 scope probe to pin 7 on RS-422 port A (PC104 board header J30). Attach channel 2 scope probe to pin 4. Pin 7 is a TDM clock signal and pin 4 is a TDM framesync signal.

You should see digital scope displays similar to Figures 16 and 17 below. The first display is for 2400 bps mode, with packed format enabled. The second display shows 1200 bps mode, also with packed format enabled.

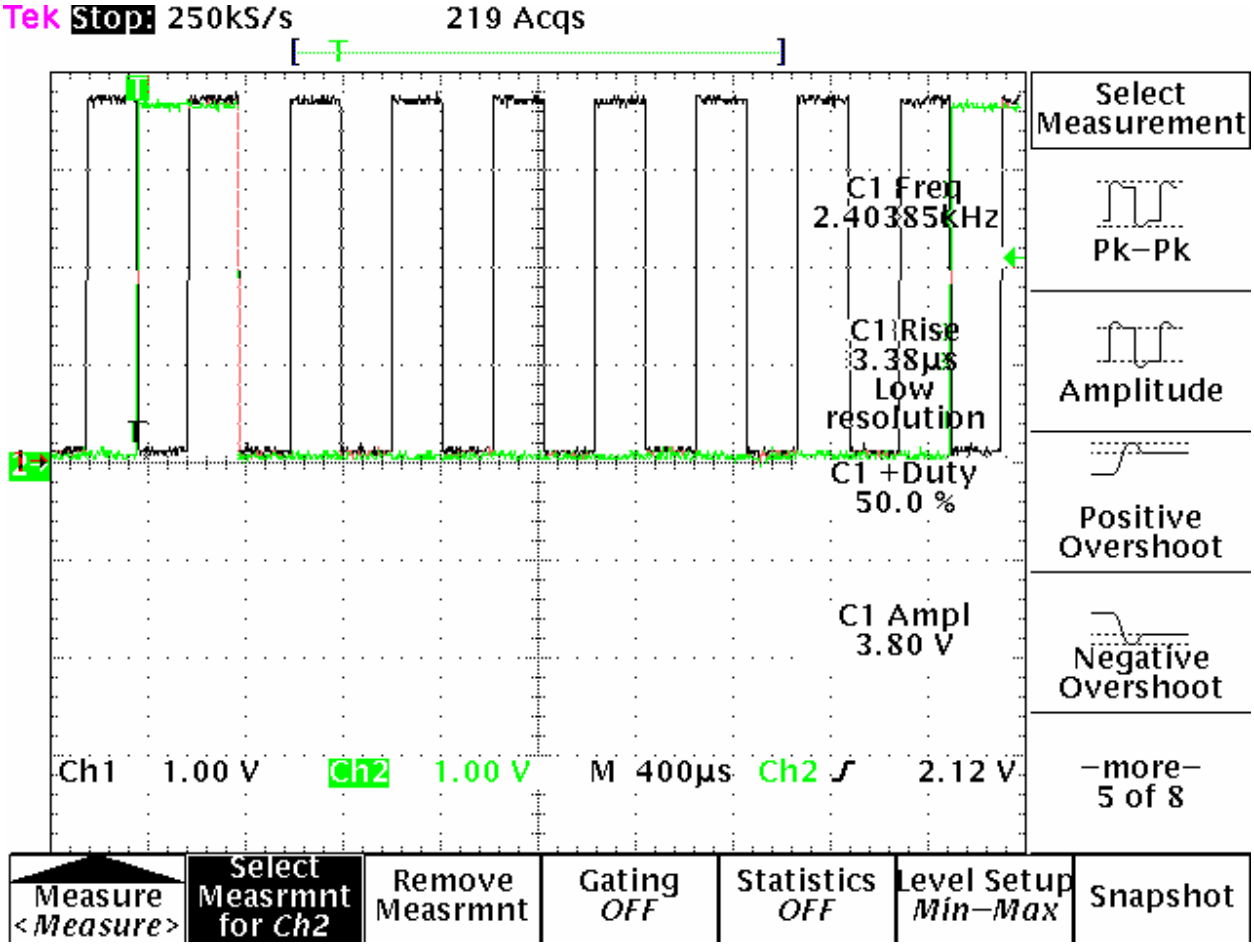


Figure 16, 2400 bps Measurement on RS-422 Port A Connector Using Digital Scope

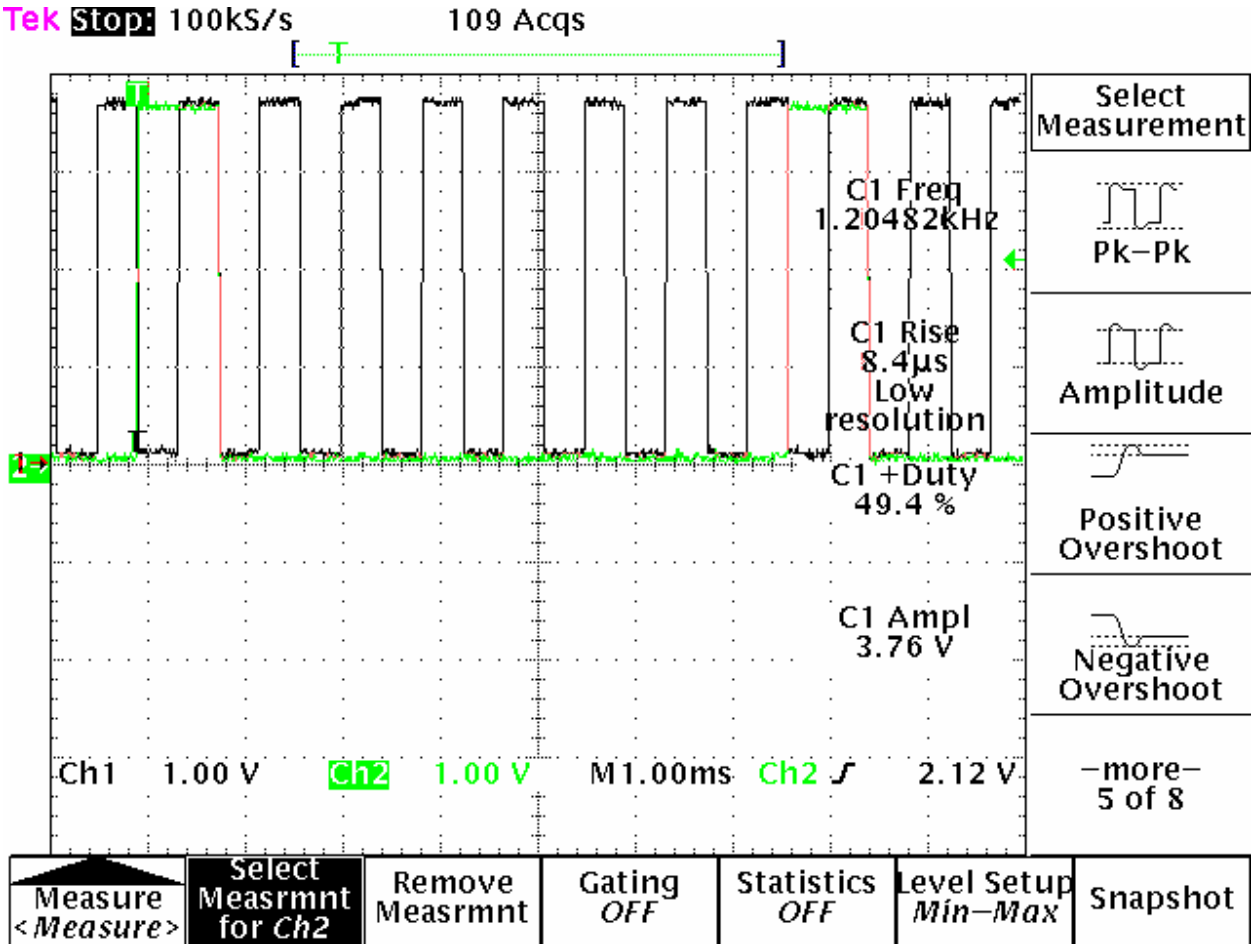


Figure 17, 1200 bps Measurement on RS-422 Port A Connector Using Digital Scope

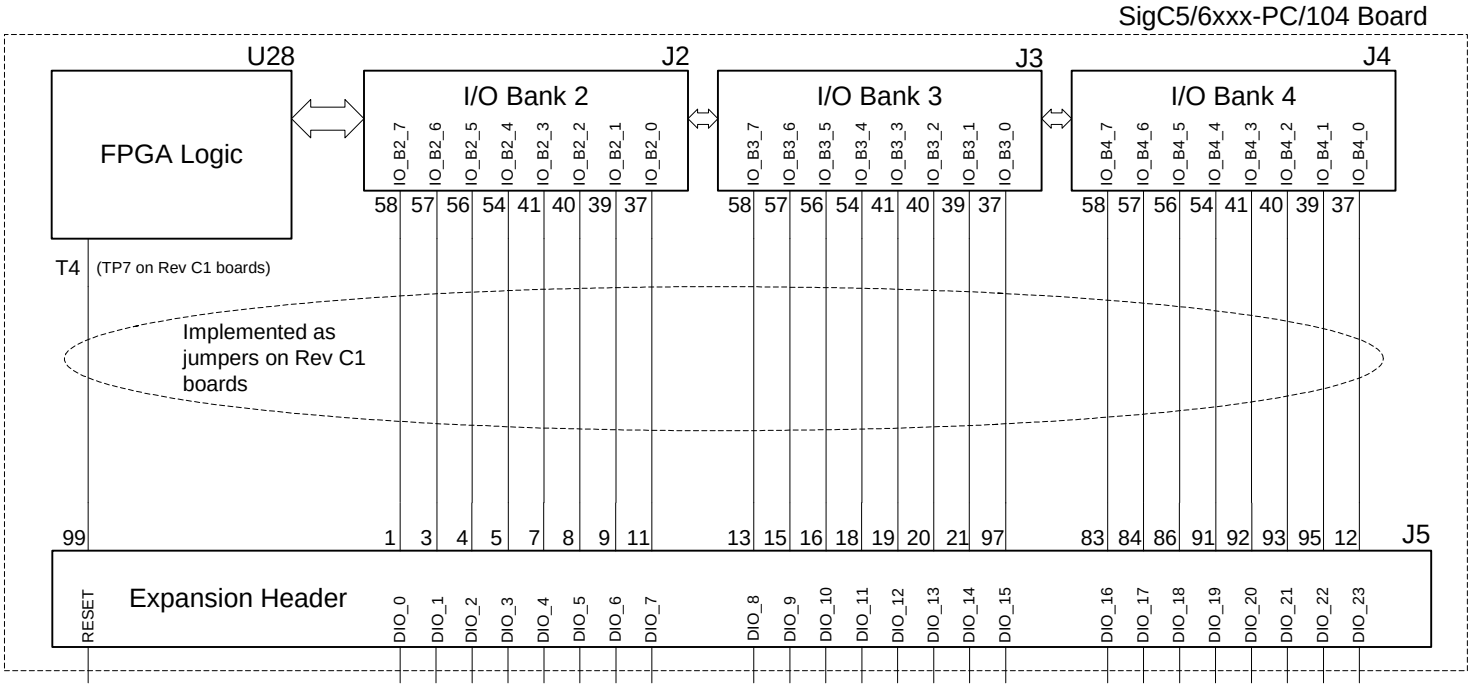
In the scope display figures above, black trace depicts clock and green trace shows the frame sync signal. In both cases, 8-bit framesync is enabled; i.e. the framesync pulse on channel 2 trace repeats every 8 clock pulses.

Statistics for the clock signal are shown at right of the display area, including frequency, rise-time, duty-cycle, and amplitude. Amplitude measurements reflect the output of the RS-422 drivers on the board.

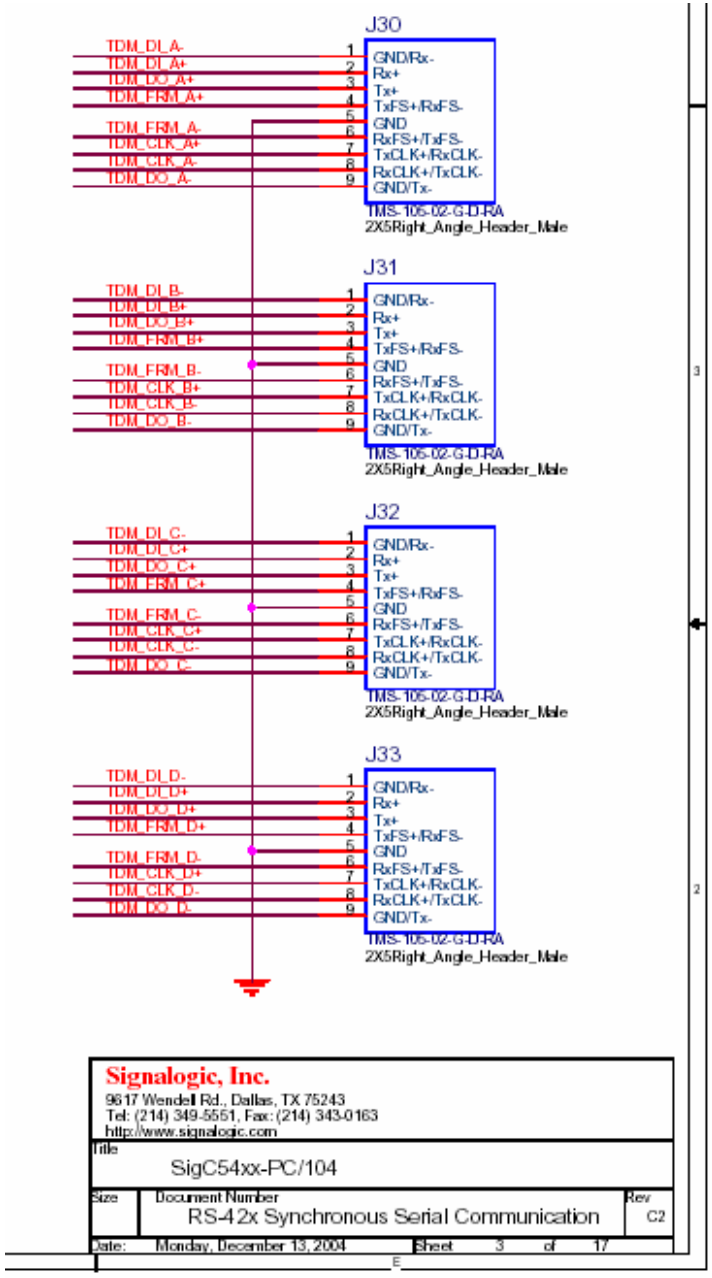
Using unpacked formats, you should be able to measure 3200 and 1659 bps rates, for MELPe bitrates 2400 and 1200 bps, respectively.

5 Appendix A, Wiring and Cabling Diagrams

Below is a diagram showing pin assignments on the J5 digital I/O header.

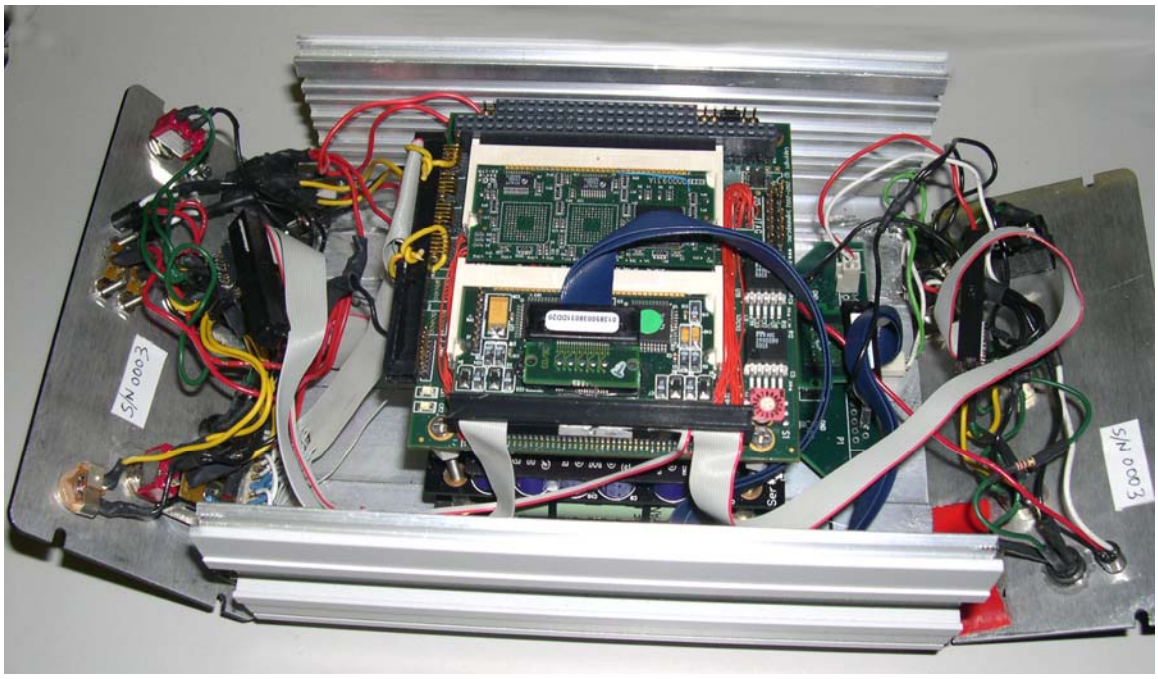

SigC5/6xxx-PC/104 Board
U28
J2
J3
J4
FPGA Logic
I/O Bank 2
I/O Bank 3
I/O Bank 4
IO_B2_7 IO_B2_6 IO_B2_5 IO_B2_4 IO_B2_3 IO_B2_2 IO_B2_1 IO_B2_0
IO_B3_7 IO_B3_6 IO_B3_5 IO_B3_4 IO_B3_3 IO_B3_2 IO_B3_1 IO_B3_0
IO_B4_7 IO_B4_6 IO_B4_5 IO_B4_4 IO_B4_3 IO_B4_2 IO_B4_1 IO_B4_0
58 57 56 54 41 40 39 37
58 57 56 54 41 40 39 37
58 57 56 54 41 40 39 37
T4
(TP7 on Rev C1 boards)
Implemented as jumpers on Rev C1 boards
99
1 3 4 5 7 8 9 11
13 15 16 18 19 20 21 97
83 84 86 91 92 93 95 12
J5
Expansion Header
RESET
DIO_0 DIO_1 DIO_2 DIO_3 DIO_4 DIO_5 DIO_6 DIO_7
DIO_8 DIO_9 DIO_10 DIO_11 DIO_12 DIO_13 DIO_14 DIO_15
DIO_16 DIO_17 DIO_18 DIO_19 DIO_20 DIO_21 DIO_22 DIO_23

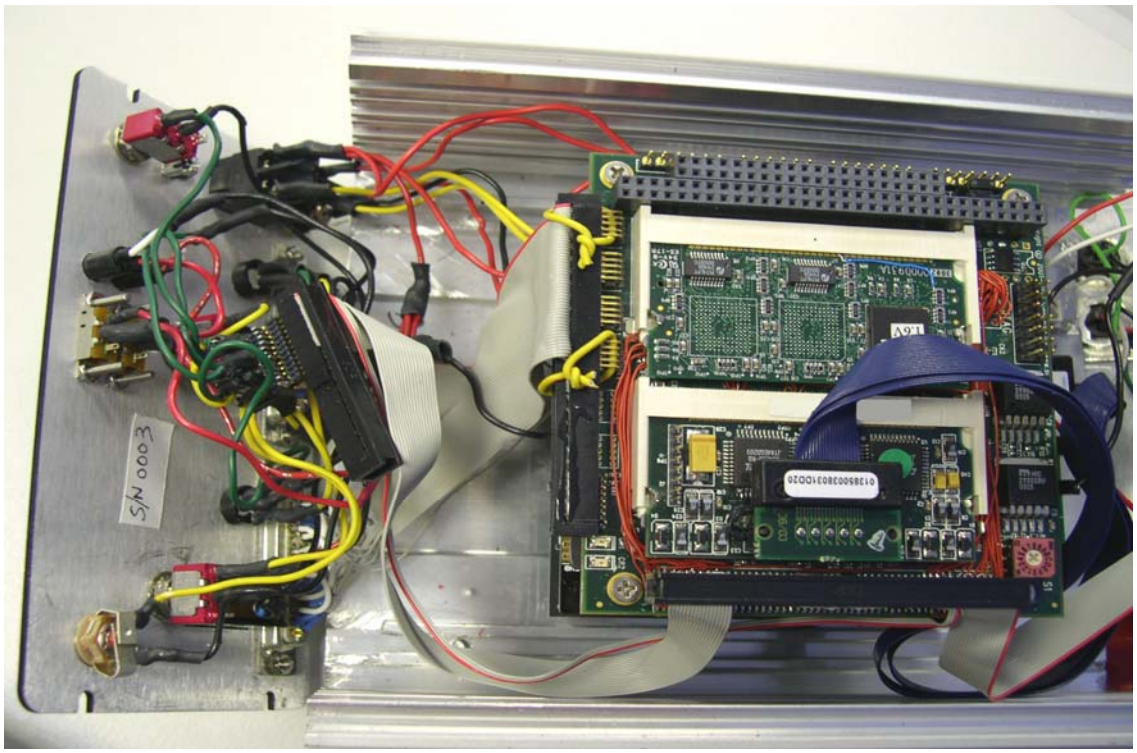
Below is a SigC5xxx-PC104 schematic excerpt showing RS-422 connector pin assignments. RS-422 Port A is located on J30, Port B on J31, and so on.

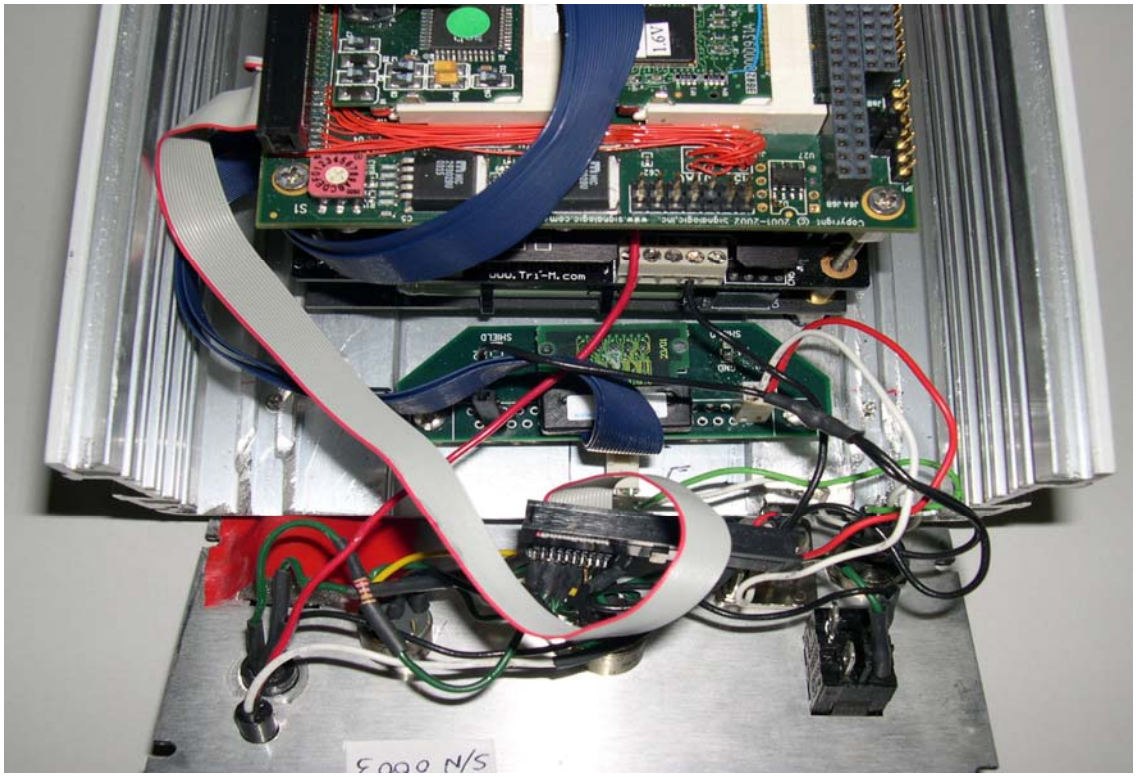

J30
TDM_DI_A-
TDM_DI_A+
TDM_DO_A+
TDM_FRM_A+
TDM_FRM_A-
TDM_CLK_A+
TDM_CLK_A-
TDM_DO_A-
GND/Rx-
Rx+
Tx+
TxFS+/RxFS-
GND
RxFS+/TxFS-
TxCLK+/RxCLK-
RxCLK+/TxCLK-
GND/Tx-
TMS-105-02-G-D-RA
2X5Right_Angle_Header_Male
J31
TDM_DI_B-
TDM_DI_B+
TDM_DO_B+
TDM_FRM_B+
TDM_FRM_B-
TDM_CLK_B+
TDM_CLK_B-
TDM_DO_B-
J32
TDM_DI_C-
TDM_DI_C+
TDM_DO_C+
TDM_FRM_C+
TDM_FRM_C-
TDM_CLK_C+
TDM_CLK_C-
TDM_DO_C-
J33
TDM_DI_D-
TDM_DI_D+
TDM_DO_D+
TDM_FRM_D+
TDM_FRM_D-
TDM_CLK_D+
TDM_CLK_D-
TDM_DO_D-
Signalogic, Inc.
9617 Wendell Rd., Dallas, TX 75243
Tel: (214) 349-5551, Fax: (214) 343-0163
http://www.signalogic.com
Title
SigC54xx-PC/104
Size
Document Number
RS-42x Synchronous Serial Communication
Rev
C2
Date: Monday, December 13, 2004
Sheet 3 of 17

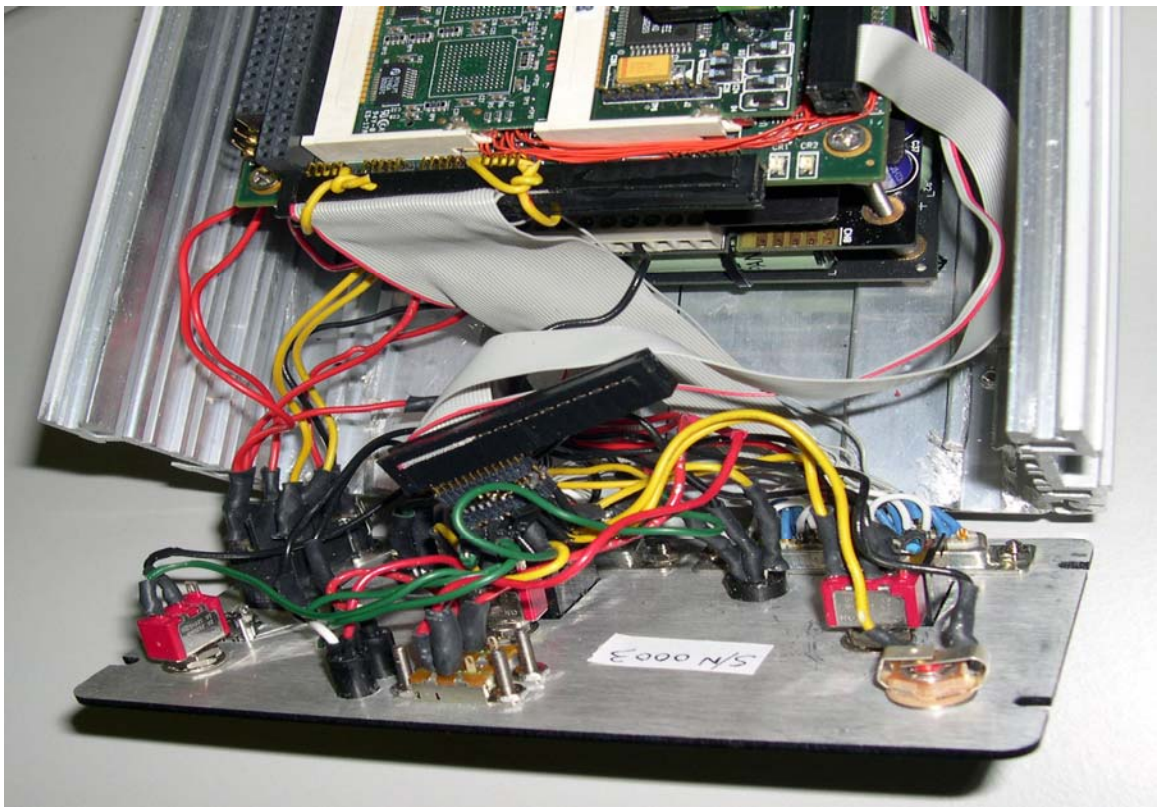
6 Appendix B, Enclosure Images

In this appendix are a series of example enclosure images intended to give some ideas for cabling and mechanical form fit when mounting the Codec-PC104 board set in a ruggedized enclosure.




S/N 0003




E000 N/S